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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,559	03/12/2004	Dustin A. Woodbury	33851/41886	6517

7590 01/31/2006

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,559	WOODBURY ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/12/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chi, U.S. Patent No. 5,173,437, in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 1, Chi discloses a method of forming a capacitor in an IC, the method comprising (See Abstract, Figs. 5-8, and depending portions of specification):

Forming a first non-single crystalline layer (first polysilicon layer 56) on a gate dielectric layer 54 of a substrate 50 of an IC;

Forming a capacitor dielectric layer (58,60) on the first non-single-crystalline layer;

Forming a second non-single-crystalline layer (second polysilicon 62) on the capacitor dielectric layer;

Removing portions of the second non-single-crystalline layer to define a top plate (70) of the capacitor (abstract);

Removing portions of the capacitor dielectric layer to define a dielectric of the capacitor (lines 17-20, Col. 4; Fig. 7);

Removing portions of the first non-single-crystalline layer to define a bottom plate (80) of the capacitor after a top plate is define (lines 35-37, Col. 4; Fig. 7).

Chi discloses the gate dielectric layer is an FOX layer formed in the substrate but fails to disclose the gate dielectric layer is a layer formed on a surface of the substrate. AAPA discloses the gate dielectric layer 26/24 formed on the surface of the substrate (Figs. 1-3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate dielectric layer on the surface of the substrate as in AAPA because the gate dielectric layer is formed at the same time with the gate dielectric layer that formed under the transistor in order to reducing the processing step and yet having similar function as FOX. The gate dielectric layer formed on the surface of the substrate is used as the gate dielectric layer for transistor and also as the insulator layer for capacitor.

Kim et al., U.S. Patent No. 5,166,090, Tseng et al., U.S. Patent No. 5,550,077, Lu, U.S. Patent No. 5,110752, Watanabe, U.S. Patent No. 6,420,222 also similar limitations of claim 1 above. Chan, U.S. Patent No. 5126280 and Rhodes et al., U.S. Patent No. 5262343 discloses the formation of gate dielectric layer on the surface of the substrate and under the capacitor.

Regarding claim 2, Chi discloses wherein portions of the first non-single-crystalline layer are removed to define a gate of a transistor of the IC (Col. 4, Fig. 7).

Regarding claim 3, Chi discloses forming a mask 64 over the second non-single-crystalline layer with an opening and etching to remove the portions of the second non-single-crystalline layer (Fig. 6).

Regarding claim 4, Chi discloses the step of etching to remove the portions of the capacitor dielectric layer using the mask (lines 17-20, Col. 4).

Regarding claim 5, Chi discloses the use of top plate as a mask and etching to remove the portions of the capacitor dielectric layer (lines 17-20, Col. 4).

Regarding claim 6, Chi discloses wherein using the top plate as a mask and etching is performed one of before and after removing the portions of the first non-single-crystalline layer (Col. 4).

Regarding claims 7-11, Chi discloses forming a mask 72 over the top plate and exposed one or more of the first non-single-crystalline layer and capacitor dielectric layer and removing portions of the capacitor dielectric layer and first non-single-crystalline layer to define the bottom plate, and using the top plate as a mask to etching

and remove additional portions of the capacitor dielectric layer to define the dielectric layer of the capacitor (Fig. 7; Col.4).

Regarding claim 12, Chi discloses forming a top dielectric layer over the first and second plates (Fig. 8) and forming contact vias to the first plate through the top dielectric and the capacitor dielectric and to the second plate through the top dielectric (Cols. 4-5).

Conclusion

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP ' 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1785.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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